## REMARKS

The present application was filed on October 31, 2003 with claims 1-20. Claims 17-19 were previously canceled. Claims 1-16 and 20 remain pending, with claims 1 and 20 being the pending independent claims.

The drawings remain objected to as being informal.

Claims 1-16 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0049564 (hereinafter "Ng") in view of U.S. Patent No. 6,665,268 (hereinafter "Sato").

In this response, Applicants again traverse the objection to the drawings, and also traverse the §103(a) rejection of claims 1-16 and 20.

With regard to the objection to the drawings, Applicants fully addressed this objection in their previous response filed March 27, 2008. However, the Examiner has apparently made an error in failing to remove the paragraph on page 2 of the Office Action that sets forth this objection. As Applicants indicated in their previous response, formal drawings have in fact been filed for this application, and the objection is therefore improper and should be withdrawn.

Applicants respectfully traverse the §103(a) rejection. Independent claim 1 recites <u>a network processor integrated circuit</u> that comprises a plurality of processor clients internal to the network processor integrated circuit, an internal memory having a plurality of memory instances, and an internal memory controller for controlling access of the plurality of processor clients to the plurality of memory instances. The claim further recites that the internal memory controller comprises a configurable switching element, with the configurable switching element being connectable between the plurality of processor clients and the plurality of memory instances and being operative to control access of particular ones of the plurality of processor clients to particular ones of the plurality of memory instances. The configurable switching element is configurable to connect any one of at least a subset of the plurality of processor clients to each of at least a subset of the plurality of memory instances. In a first selectable configuration of the configurable switching element, a given one of the processor clients is permitted to access a first set of memory instances comprising one or more of the plurality of memory instances, and in a second selectable configuration of the configurable switching element,

the given processor client is permitted to access a second set of memory instances comprising one or more of the plurality of memory instances, the second set being different than the first set.

It is important to note that the claim expressly recites that the plurality of processor clients, the plurality of memory instances, and the internal memory controller with configurable switching element having first and second selectable configurations are <u>all within the recited network processor integrated circuit itself</u>.

An illustrative embodiment of the claimed arrangement is shown in FIG. 1 of the drawings. There, a network processor 102 comprises processor clients 120, memory instances 122 of an internal memory 104, and a memory controller 115. As in the above-noted limitations of claim 1, the processor clients 120, the memory instances 122 and the memory controller 115 are <u>all internal to the network processor 102</u>. See the specification at, for example, page 5, lines 7-12. The specification at page 1, lines 10-13 indicates that a network processor generally controls the flow of packets between a physical transmission medium and a switch fabric in a router of other type of packet switch. The specification further makes clear that the above-described illustrative network processor 102 may be configured as an integrated circuit to provide an interface between a network and a switch fabric in a router or switch. See the specification at, for example, page 14, lines 12-13.

The collective teachings of Ng and Sato clearly fail to disclose or suggest a network processor integrated circuit having as internal elements thereof the recited processor clients, memory instances and memory controller with configurable switching element having first and second selectable configurations as recited.

The Examiner in formulating the §103(a) rejection of claim1 fails to address the network processor integrated circuit limitations of the claim. Instead, the Examiner refers to claim 1 as simply "an apparatus." See the final Office Action at page 2, last two lines, and page 3, first two lines. However, what is claimed is not an apparatus generally, but a particular type of apparatus, namely <u>a network processor integrated circuit</u>. As noted above, the specification indicates that a network processor is a particular type of processor, one that generally controls the flow of packets between a physical transmission medium and a switch fabric. Neither Ng nor Sato disclose such a network

processor implemented as an integrated circuit and having as internal elements of said integrated circuit the recited processor clients, memory instances and memory controller with configurable switching element having first and second selectable configurations.

The Examiner relies primarily on the arrangement shown in FIG. 2 of Ng and the corresponding text in paragraphs [0036] through [0039]. However, this figure shows a storage area network (SAN) that connects multiple server devices 202 with multiple storage devices 230-238. It is clear from, for example, paragraph [0001] of Ng that a given SAN and its associated server devices and storage devices are not elements of a network processor integrated circuit.

The Examiner apparently acknowledges these fundamental deficiencies of Ng as applied to claim 1, but argues that any missing teachings can be found in Sato in FIGS. 9A and 9B and columns 25 and 26. See the final Office Action at page 4, first paragraph. However, the crossbar network unit 10 as shown in the relied-upon figures is part of "a parallel processor system," further described in Sato as "a kind of supercomputer," and not part of a network processor integrated circuit of the type recited in the claim. See Sato at column 11, lines 48-57. Moreover, the crossbar network unit 10 is operative to interconnect an arbitrary set of the processor elements of the parallel processor system with one another for purposes of load testing the parallel processor system. See Sato at, for example, column 12, lines 15-29, column 12, line 56, to column 13, line 10. Accordingly, the crossbar network unit 10 is not an element of a network processor integrated circuit, nor is it configurable to connect processor clients of such a network processor integrated circuit to internal memory instances of such a network processor integrated circuit, as recited.

It is therefore clear that the collective teachings of Ng and Sato fail to meet the limitations of claim 1.

The Examiner further argues that it would be obvious to combine Ng with Sato to meet the claimed arrangement. However, as indicated above, the relied-upon portions of Sato teach the use of a crossbar network unit 10 for interconnecting processor elements of a parallel processor system with one another. The relied-upon portions of Ng, on the other hand, disclose a SAN that connects multiple server devices 202 with multiple storage devices 230-238. It is not clear why one skilled in the art would be motivated to

adapt the crossbar network unit 10, utilized in Sato to interconnect supercomputer processor elements with one another for purposes of load testing, to communication between server devices and storage devices in a SAN of the type disclosed in Ng.

The Examiner argues that such a combination would be obvious because it "would decrease the delays in communication between the client and the memory . . . caused by physical distance between the devices." See the final Office Action at page 4, first paragraph. However, the portion of Sato at column 2, lines 38-43, cited in support of this alleged motivation involves a parallel processor system or supercomputer in which the various processor elements may be separated from one another by large physical distances. The present invention, by way of contrast, involves a network processor integrated circuit in which the processor clients are internal to that integrated circuit. In this integrated circuit context, there is no significant physical distance between the various processor clients, and as a result the alleged motivation is deficient. Moreover, as indicated above, Ng deals with communications between server devices and storage devices in a SAN, and Sato deals with interconnecting processor elements of a parallel processor system or supercomputer for purposes of load testing. These are entirely different systems, and there does not appear to be any need whatsoever for the type of load testing disclosed in Sato within the SAN of Ng.

Applicants therefore respectfully submit that the statements proffered by the Examiner fail to provide sufficient objective motivation for the combination and, rather, are conclusory statements of the sort rejected by both the Federal Circuit and the U.S. Supreme Court. See KSR v. Teleflex, 127 S. Ct. 1727, 1741 (2007), quoting In re Kahn, 441 F. 3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

Independent claim 20 is believed allowable for reasons similar to those identified above with regard to claim 1.

Dependent claims 2-16 are believed allowable at least by virtue of their dependence from claim 1, and are also believed to define separately patentable subject matter relative to the proposed combination of Ng and Sato.

In view of the above, Applicants believe that claims 1-16 and 20 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejection.

As indicated previously, a Notice of Appeal is submitted concurrently herewith.

Respectfully submitted,

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Enclosure(s): Notice of Appeal